# Design of Multiplierless Multiple Constant Multiplication for Convolution Circuit

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# Abstract:

A radix-3 partitioning scheme can provide the pre-multiplication factors for natural numbers, which they engaged to construct a convolution circuit i.e. used for multimedia and filtering applications. In proposed method, the partitioned unsigned integer input is multiplied with 32-bit floating point filter coefficient. Ancient architectures like distributed arithmetic, shifters, recoding circuitry and other multiplier circuits are substituted with ROMs and floating point adders used for improving the efficiency. In floating point inputs, for mantissa addition the carry save adder can be substituted by parallel prefix adder. Subsequently, derived from the multiplied result it led to less area occupation. The obtained results are simulated by Xilinx ISE and compared for betterment of area, power and delay with the former approaches

**Tools used:**

**Xilinx 13.2**